Các bài về watch point: The following sequence of instructions are executed.

1. What is the correct value of AX, DX at watch point?

MOV DL,FF

MOV AL,42

IMUL DL

watch point:

DA: FFFFx42

AX = FFBE = FFFFx42

DX=00FF

1. What is the correct value of flag bits at watch point?

MOV AL, 0F

ADD AL, F1

watch point:

Da: Zero flag (OF) = set

Carry flag (CF) = set

1. The following sequence of instructions are executed. What is the correct value of CF and OF at  
   watch point?  
   MOV AX,140h  
   MOV CX,8h   
   MUL CX  
   watch point:  
    DA: CF= reset  
    OF= reset
2. What is the correct value of AX, CX, DX at watch point?  
   MOV AX,30  
   MOV CX,FFFF  
   MUL CX  
   watch point:  
    DA: CX = FFFF  
    AX = FFD0  
    DX 002F
3. What is the correct value of flag bits at watch point?

MOV AL,-5  
SUB AL,124

1

1111 1011

0111 1100

0 0111 1111  
watch point:  
DA: Zero flag (OF) = 0  
 Overflow flag (OF) = set  
 Sign flag (SF) =0  
 Carry flag (CF) = 0

1. What is the correct value of AX, DX at watch point?  
   MOV DL,FF  
   MOV AL,42  
   IMUL DL  
   DA: AX = FFBE  
    DX=FFFF
2. The following sequence of instructions are executed. What is the correct value of CF and  
   OF at watch point?  
   MOV AX,FFF6h  
   MOV CX,1000h  
   IMUL CX  
   watch point:  
   DA: OF= set  
    CF= set
3. . The following sequence of instructions are executed. What is the correct value of flag bits at  
   watch point?  
   MOV AX,FFFF  
   MOV CX,5  
   MUL CX  
   watch point:  
   DA: Carry flag (CF) = set  
    Overflow flag (OF) = set
4. The following sequence of instructions are executed. What is the correct value of flag bits at  
   watch point?  
   MOV AL, 80h  
   MOV BL, 2h  
   MUL BL  
   watch point:  
   DA: Overflow flag (OF) = set  
    Carry flag (CF) = set
5. The following sequence of instructions are executed. What is the correct value of flag bits at  
   watch point?  
   MOV DL,FF  
   MOV AL,F6  
   IMUL DL  
   watch point:  
   DA: OF = 0  
    CF = 0
6. . The following sequence of instructions are executed. What is the correct value of flag bits at watch point?  
   MOV AL, 0F  
   ADD AL, F1  
   watch point:  
   DA: Zero flag (OF) = set  
    Carry flag (CF) = set
7. . The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point? MOV AX,0020 MOV CX,0010 MUL CL watch point:

ĐA: AX = 0200

DX 0000

CX = 0010

1. Select correct match for AL and carry flag at watch point #1:  
   MOV BL, 8C  
   MOV AL, 7E  
   ADD AL, BL  
   watch point #1:  
   DA: Carry flag set

AL 0A

Các bài về chia:

1. Select the correct sequence of instructions to compute -1024/128 (all values are in hex).

Step 1: mov ax, fc00

Step 2: cwd

Step 3: MOV CX,80

Step 4: IDIV CX

1. A system programmer needs to divide ­-6247 by 300 (decimal)

MOV AX,E799;

CWD; chuyển số AX từ dương sang âm, FFFFE799

MOV BX, 12Ch

IDIV BX;

# Ôn kiến trúc máy tính:

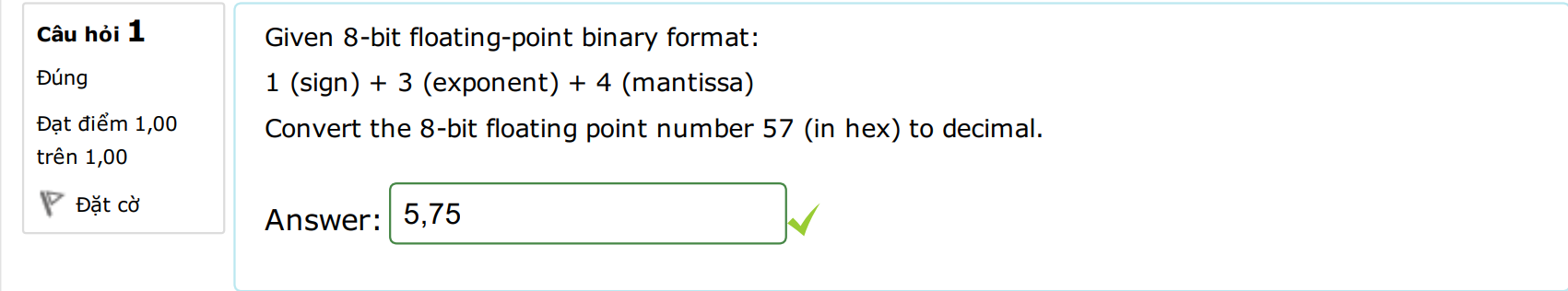
Lệnh:

Test instruction: To test one bit in a byte without destructing the byte

CMP instruction: to compare source and destination operands by compraring

AND instruction: To isolate one or more bits in a byte value

Một số bài tập giải được



Giải:

5716 = 0|101|0111

1102=6, 5-3=2

1.01112\*22=101.112

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 22 | 21 | 20 | 2-1 | 2-2 |
| 1 | 0 | 1 | 1 | 1 |
| 4 |  | +1 | +0.5 | +0.25 |
|  |  |  |  | 5.75 |

1. Physical address of the stack pointer is 2DA82, stack segment located at 1DAE. Computer the value of SP register? DA: FFA2

1DAE \* 10h + FFA2 = 2DA82

⬄ 7598 \* 16 + 65442 = 187010

1. Select correct match for AX (Decimal) at watch points:

MOV AX, 1BC

MOV CL, 2

SHL AX, CL

watch point #1:

ADD AX, 166

watch point #2:

SHR AX, CL

SHR AX, CL

......

watch point #1: 1776

watch point #2: 942

watch point #3: 485

2. Which could be correct ones for the destination operand in a data movement instruction?

Select one or more:

immediate data, register, memory location

3. Structural components of computer include:

-> IO device, central processing unit, memory, interconnection

4. Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 00 40 08 42 - 99 80 3E 20 99 00 75 24

SI = 120 bỏ 4 số từ 13 lấy 4 số(+4)

124 = 42084000

The following instruction is executed: MOV EAX, [SI+4]

Assume the value in EAX is a 32-bit floating-point binary, what is the value of EAX in decimal?

🡪 EAX = 42084000

5. Write mask byte (in hex) to set higher 4 bits in a byte value with OR instruction (LSB is the 1st bit).

🡪 F0

6. After executing PUSH EAX instruction, the stack pointer:

🡪 decrement by 4

7. Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.

🡪 80

8. The instruction that subtracts 1 from the contents of the specified register/memory location is

🡪 DEC

9. What is the meaning of Amdahl's law in processor performance evaluation?

🡪 the potential speedup of a program using multiple processor compared to a single processor.

10. Which are the correct actions for LODSW string operation if DF is reset (=0)

🡪 increase SI by 2

Load 16-bit value at memory location pointed by DS:[SI] into AX

11. the instruction, CMP to compare source and destination operands by

🡪 subtracting

12. To balance the super speed of CPU with the slow response of memory, which of the following measures have been made by engineers in system design?

🡪 Make use of both on-chip and off-chip cache memory

Make wider data bus path

Using higher-speed bus and us hierarchy

14. Select correct match for register values at watch points:

MOV AX, 152D

ADD AX, 003F

watch point #1:

ADD AH, 10

watch point #2:

🡪

watch point

#2: AH = 25

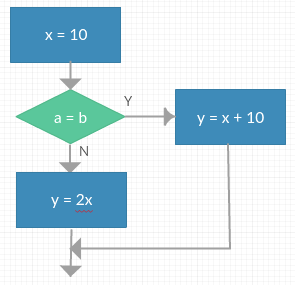
watch point

#1: AL = 6C

16. After executing the POP EAX instruction, the stack pointer

🡪 increments by 4

18. Given a flowchart of an algorithm:



mov dl,10  
cmp al,bl  
jnz n\_label  
add dl,10  
jmp e\_label  
n\_label:  
mov cl,1  
shl dl,cl  
e\_label:  
mov dh,dl

19. Given a code snippet:

int n = 10;

do {

n--;

} while (n > 0);

Which ones are the equivalent logic sequence of instructions in Assembly

🡪mov cx, 10  
a\_label:  
.....  
loop a\_label

mov cx, 10  
a\_label:  
.....

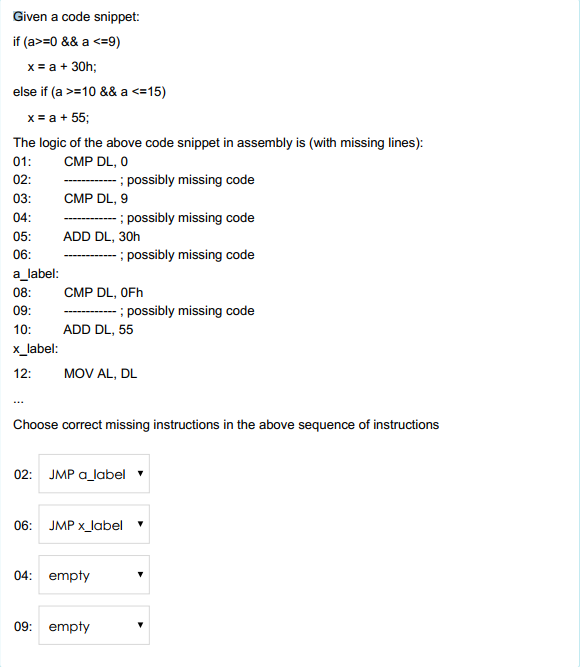
dec cx  
jnz a\_label

20. The instruction, MOV AX, 0005h belongs to which addressing mode?

🡪Immediate

21. Which are valid based indexed addressing?

🡪 [BX][SI]

22. 

02: jl xlabel

04:jg a\_label

06: jmp x\_label

09: jg x\_label

23. Enter debug command to fill 256 bytes in data segment starting from 100 with value 0D

🡪Answer: F 100 1FF 0D

24. Which of the following instructions are not valid?

MOV DS, B800h

25. Which one best describe cache hit and cache miss?

Cache miss ratio 🡪 the number of memory accesses that CPU must retrieve from the main memory per the total number of memory accesses

Cache hit ratio 🡪 the number of memory accesses that the CPU can retrieve from the cache per the total number of memory accesses

26. For cache write policies, which are often used for write­hit and write­miss

Write­hit 🡪 Write­back

Write­miss 🡪 Write­allocate

27. Choose correct features for SRAM and DRAM

DRAM 🡪 Slower access time, cheaper cost per bit, can manufacture with larger size

SRAM 🡪 Faster access time, cost more per bit, smaller size

28. Identify the correct sequence to update a page onto a flash memory?

Step 1🡪 the entire block is being read from flash into RAM then request data in page is update

Step 2🡪 the entire block of flash memory are erased

Step 3🡪 The entire block from RAM then is written back to the flash memory

29. Choose correct set of registers for x86 processor

Data pointer to source memory in extra segment ES: SI

Pointer to variable in stack SS: BP

Instruction pointer CS: IP

Data pointer in data segment DS: BX

30. Match the definition of flag bits in PSW

contains the carry of 0 or 1 from the leftmost bit after an arithmetic operation CF

determine the direction for moving or comparing data between memory areas DF

determine whether an external interrupts are to be ignored or processed IF

the processor switches to single­step mode TF

31. Which is not correct about MOORE law?

🡪The number of transistors that could be put on a single chip was triple every year nowadays.

Likely triple after 2000

32. For better speed, in CPU design, engineers make use of the following techniques:

🡪Branch prediction

Pipelining

Speculative execution

33. To balance the super speed of CPU with the slow response of memory, which of the following measures have been made by engineers in system design?  
Select one or more:

🡪  
Make wider data bus path  
Make use of both on­chip and off­chip cache memory  
Using higher­speed bus and us hierarchy

35. What are the processor's instruction categories

🡪 Data processing  
Control

Processor ­ I/O  
Processor ­ Memory

36. In computer, how does the processor serve multiple interrupt request from devices?

🡪 Each device are assigned an interrupt priority, the device with lower priority will be served.

37. Bus is a shared transmission medium, multiple devices connect to it but only one at a time can successfully transmit. Which component in computer facilitates this operation?  
🡪 Bus Arbiter

38. When many devices of different transmission speed connect to the same bus, the overall system performance suffers. How did the design engineers resolved this:

🡪 Multiple­Bus hierarchies

39. What are the features of direct­mapping cache organization?

🡪 Thrash ­­> low hit ratio

Simple and inexpensive

40. Which ones are not correct for static RAM?

🡪 Cheaper than dynamic RAM because simpler chip controller  
Cost per bit is lower than dynamic RAM

faster than dynamic RAM because they are made from capacitor

41. Which one is not correct?

🡪 EEPROM is erasable by exposing under UV

EPROM is erasable electrically  
Flash memory can only be erased electrically byte by byte

42. Which statements are correct for HDDs?

🡪 a. Bits are stored on tracks.  
b. Head, Track, Sector are key parameters for access data on hard disk.

43. What is correct about the function of TRIM command in SSD?

🡪 Allow OS to notify SSD the presence of occupied blocks of data which are no longer in use and can be erased internally

44. Which set of registers are valid for addressing a memory location?  
🡪 DS:SI

DS:BX

CS:IP

45. Which are valid based index addressing?

🡪 [BX+SI]

[BX+DI]

46. Which are valid index addressing?

🡪 [SI]

[BX]

[BP]

47. Which are correct about the data registers of IA­32 processors:  
🡪 Lower halves of the 16 ­registers an be used as 8­bit data registers: AH,AL,BH,BL,CH,CL,DH,DL.

Complete 32­ bit registers: EAX, EBX, ECX, EDX

Lower halves of the 32 ­registers an be used as 4 16­ bit data registers: AX,BX,CX,DX

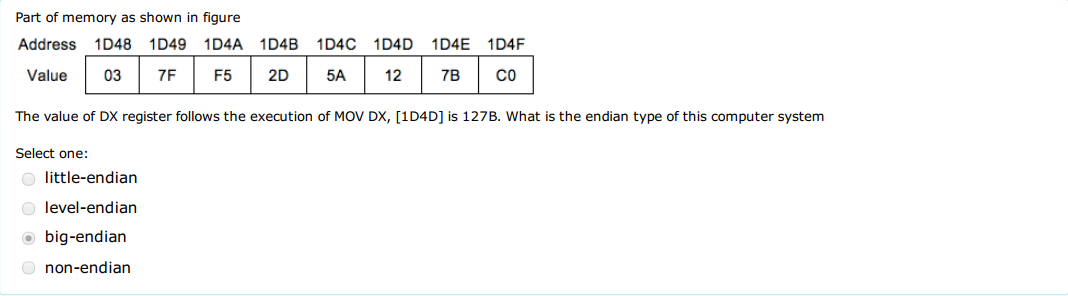
48. Which are correct about 32 bit index registers of IA­32 processors:  
Select one or more:  
🡪 EDI: 32 bit pointer to destination memory in data movement instructions

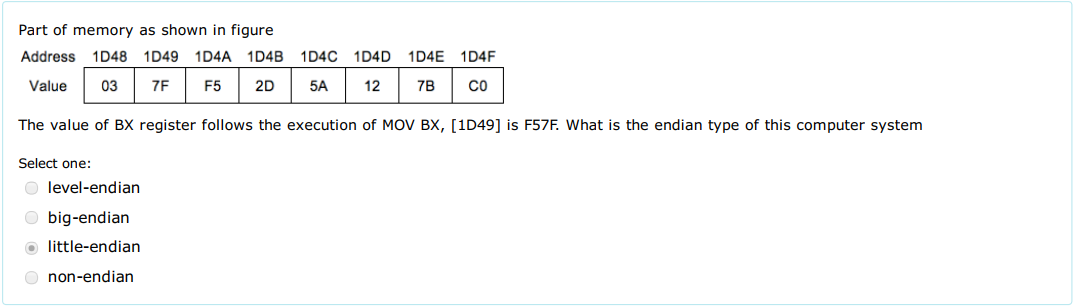
DI: 16 bit pointer to destination memory in data movement instructions

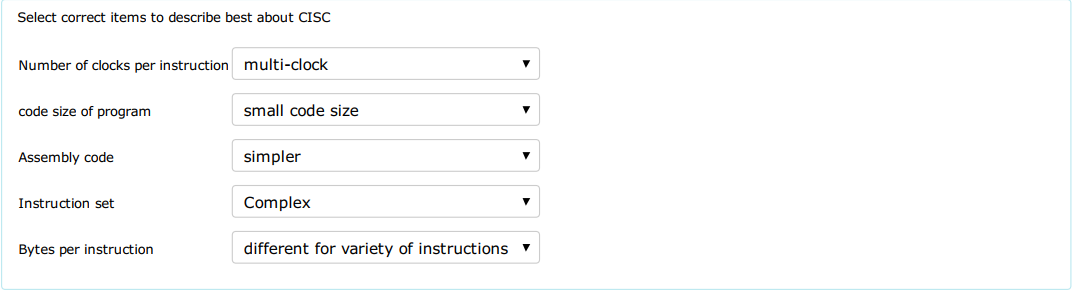
SI: 16 bit pointer to source memory in data movement instructions  
ESI: 32 bit pointer to source memory in data movement instructions

49. Which statement is correct about interrupt vector table?  
Select one or more:  
🡪 Take up 1024 bytes in the main memory

Store in the beginning area of the main memory

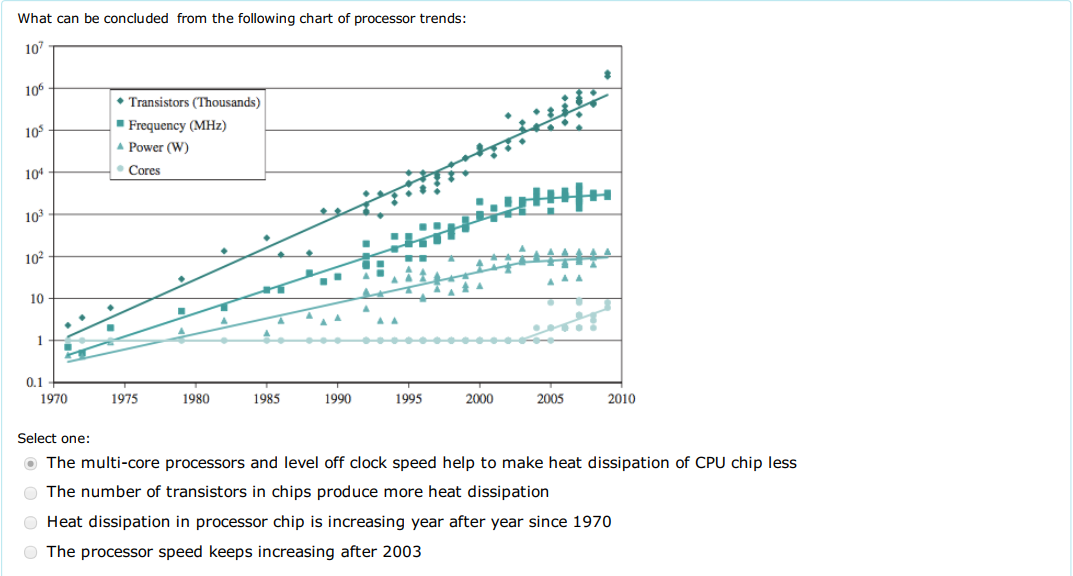
50. 

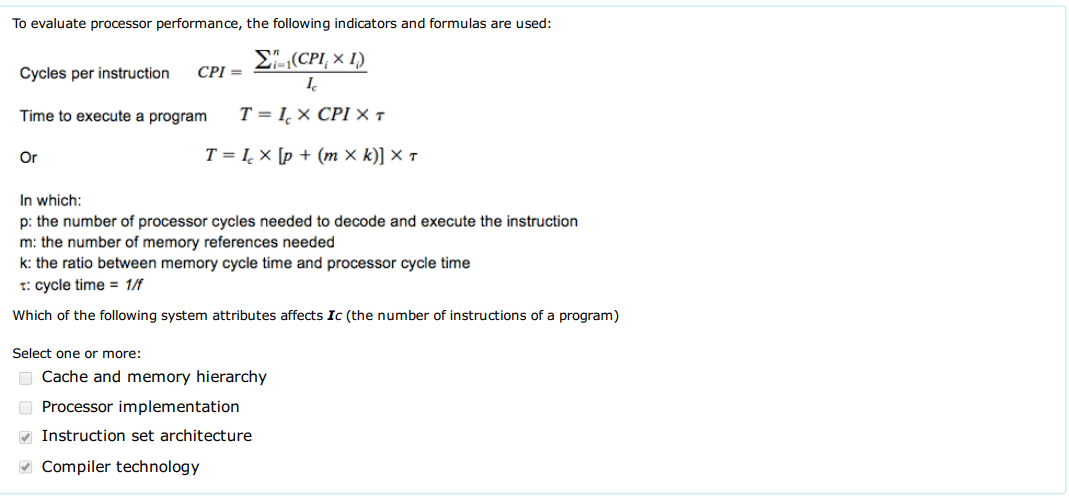
60. 

61. 

62. What best describe the Spatial and Temporal Locality?  
🡪 Temporal locality: be exploited by keeping recently used instruction and data in cache memory and by exploiting a cache hierarchy

Spatial locality: be exploited by using larger cache blocks and by incorporating prefetching mechanisms into the cache control logic

63. 

64. 

65. To evaluate processor performance, the following indicators and formulas are used:  
Which of the following system attributes affects cycle time τ  
🡪 Processor implementation

Cache and memory hierarchy

66. Key parameters to consider when evaluating processor hardware include:  
🡪 reliability

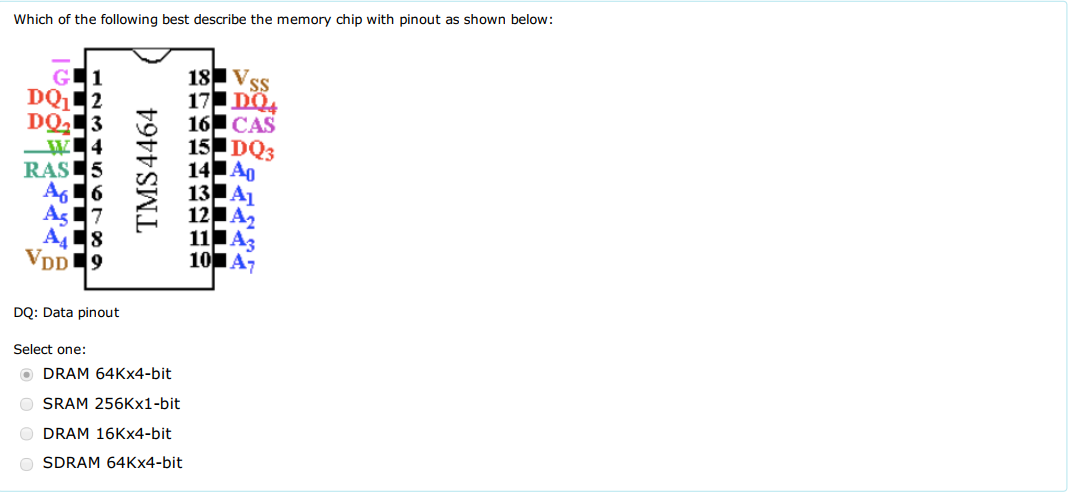
Performance

Power consumption

Size

Cost

67. A memory chip has 12 address pins, determine the maximum memory words of this chip?  
🡪 4096

68. 

Nếu ko có RAS,CAS thì đáp án là 2^8 x 4bit= 256x4bit

Nếu có thì đáp án là 2^16=64kx4bit

69. 

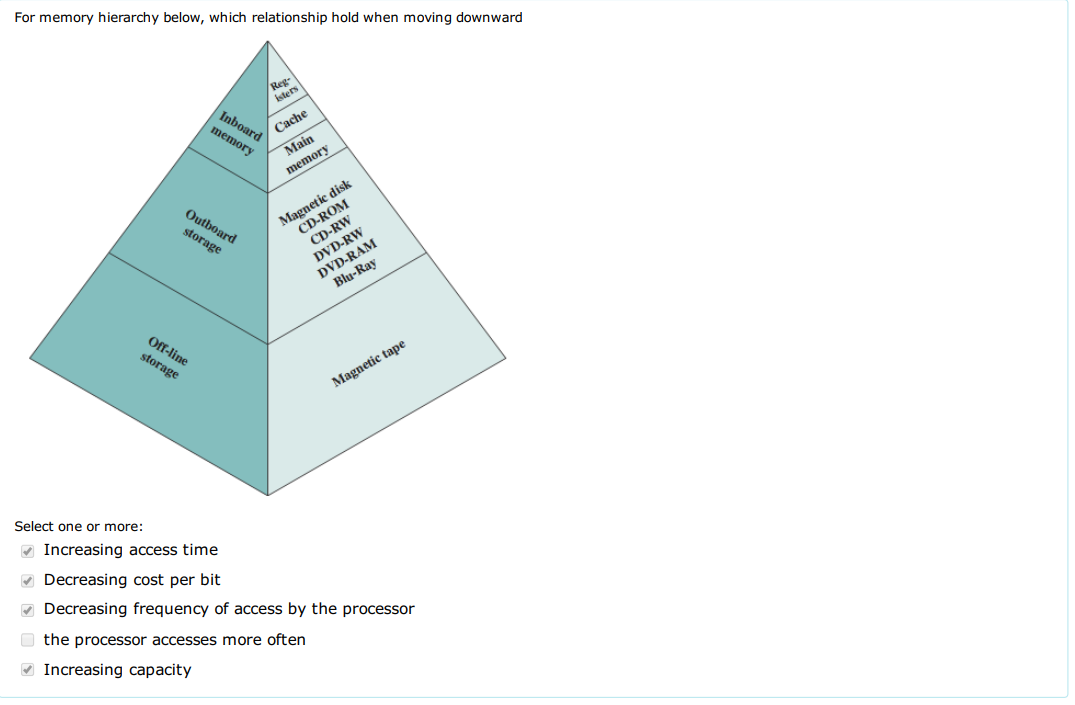
70. The three key characteristics of memory are: capacity, access time and cost. Which of the following relationships hold for a variety of memory  
technologies?  
🡪 Faster access time, greater cost per bit

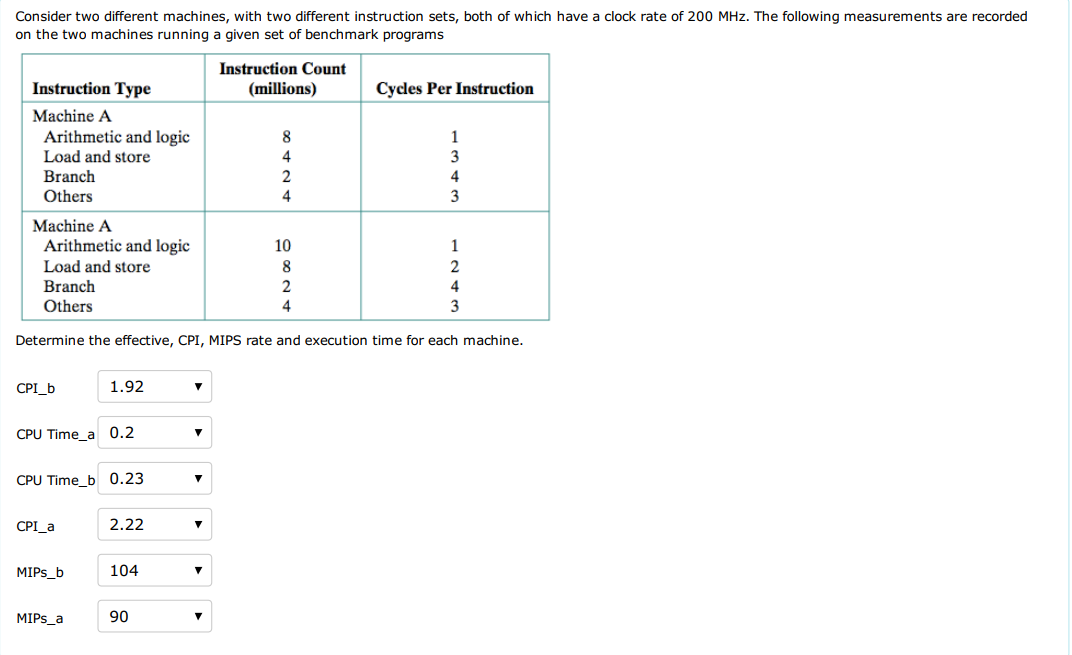
Greater capacity, smaller cost per bit

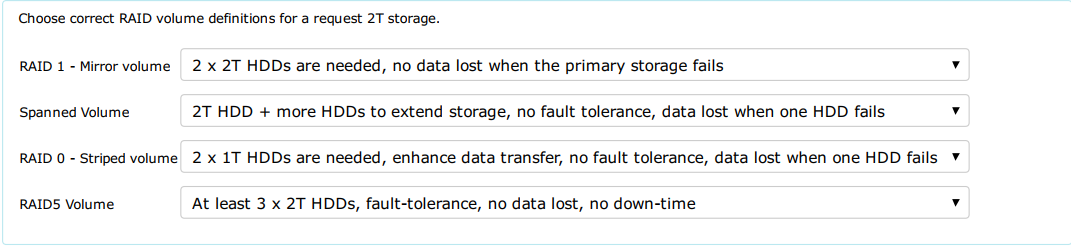
Greater capacity, slower access time

71. A SRAM memory chip labeled 32 x8bit. Which of the following is correct pinout regarding address and data lines?  
🡪 15 address pins, 8 data pins

72. In the interconnection system, the number of address lines are governs by  
🡪 CPU

73. 

74. 

75. 

76. Consider a 32­bit microprocessor whose bus cycle is the same duration as that of a 16­bit microprocessor. Assume that, on average, 30% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 30% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32­bit microprocessor?  
Select one:  
23%

80. Which of the following instructions are not legal addressing?

DA : MOV AX, [BX+SP]  
 MOV AX, [SP+1]

81.Consider the following assembly instruction sequence  
CMP DL, 0  
JB x\_label // DL=0xFF, nếu JB thì ko nhảy, nếu dùng lệnh JL thì nhảy   
CMP DL, 9  
JA a\_label  
ADD DL, 30h  
JMP x\_label  
a\_label:  
CMP DL, 0Fh  
JA x\_label  
ADD DL, 31h  
x\_label:  
MOV AL, DL  
watch point:  
Choose correct value of AL register at watch point for different value of DL?  
 DA : DL=55h 55h  
 DL=0FFh 41h  
 DL=10 38h

85. the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is

DA: REP

87. What is the meaning of Amdahl's law in processor performance evaluation?   
DA: the potential speedup of a program using multiple processor compared to a single processor

91. In the RCR instruction, the contents of the destination operand undergoes function as  
DA: carry flag is pushed into MSB then LSB is pushed into carry flag

92. Which are the correct actions for SCASW string operation if DF is set (=1)  
DA: Decrease DI by 2  
 Compare the value in AX register with 16-bit value at the memory location  
 Pointed by ES:[DI] and set/clear flag bits accordingly

93. What is the correct value of SI, AL (in hex) at watch point:  
01: MOV SI, 300h  
02: MOV AL, 10h  
03: MOV CX, 7  
04: Loop\_label:  
05: MOV [SI], AL  
06: ADD AL,10h  
07: INC SI  
08: LOOP Loop\_label  
DA: SI = 307h  
 AL = 80h

98. Which of the following is not a data copy/transfer instruction?  
Select one or more:  
DA: ADC  
 DAS

100. Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st bit).

11101001  
DA: E9

101. if the location to which the control is to be transferred lies in a segment other than the current one, then the jump instruction is call  
DA: intersegment mode

105. The instruction that supports addition when carry exists is

DA: ADC

110. Choose correct features for SRAM and DRAM  
DA:

SRAM: Faster access time, cost more per bit, smaller size

DRAM: Slower access time, cheaper cost per bit, can manufacture with larger size

113. Which are correct action for STOSB string operation if DF is reset (=0)

DA: Store 8-bit value from AL into memory location pointed by ES:[DI]  
 Increase DI by 1

114. What are components of Von Neumann, namely IAS computer?

DA: I/O Equipments

CPU

Memory

115. The instruction that is used for finding out the codes in case of code conversion problems is

DA: XLAT

117. Which are correct action for LODSB string operation if DF is reset (=0)

DA: Load 8-bit value at memory location pointed by DS:[SI] into AL

increase DI by 1

118. The instruction, MOV AX, 0005h belongs to which addressing mode?

DA: immediate

119. In multiplication instruction, when the source operand is 16 bit, how can the result be taken?

ĐA: from DX:AX

120. Hereafter is instruction sequence to compute the sum of 8 bytes starting at memory address 200. Two lines of code are possibly missing. Choose correct one to fill in?

01: \_\_\_ MOV [SI],200\_\_\_; possibly missing code

02: MOV AL, 0

03: MOV CX, 8

04: Loop\_label:

05: \_ \_CWD\_\_; possibly missing code///

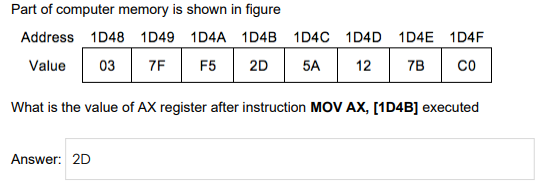
06: ADD AX, [SI];

07: INC SI

08: LOOP Loop\_label

121. In multiplication instruction, when the source operand is 8 bit, \_\_AL\_\_ will be multiplied with source.

//122.



AX=5A2D

124. Which set of registers are valid for addressing a stack memory location? SS:SP, SS:BP

125. Basic functions that a computer can perform including:

Data movement, Control, Data processing, Data storage

//127. What is the correct sequence of instruction cycle?

Step 3 Calculate operand address

Step 2 Decode Step

Step 5 Execution

Step 4 Fetch operand

Step 1 Fetch opcode

Step 6 Store result